

REMARKS

Claims 49, 57, 60, 61 and 69 have been canceled and claims 50-56, 58, 59 and 62-68 have been amended. Claims 50-56, 58, 59 and 62-68 are pending in the application. Reconsideration of the application is requested in view of the amendments and the remarks to follow.

Claims 49, 50, 53, 55, 56 and 61-63 stand rejected under 35 U.S.C. §102(e) as being anticipated by Yu et al., U.S. Patent No. 6,376,877. Claims 49, 51, 58, 61, 62, 66 and 68 stand rejected under 35 U.S.C. §102(e) as being anticipated by Ding et al., U.S. Patent No. 6,214,667. Claims 49, 50, 53, 58, 59, 61, 63 and 66 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hsieh et al., U.S. Patent No. 6,153,494. Claims 52, 54, 57 and 64 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yu et al. and Shirai et al., IEDM 1995, IEEE Cat. No. 0-7893-2700-4. Claims 52, 54, 65 and 69 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ding et al. and Shirai et al. Claims 52, 54, 60, 64 and 67 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh et al. and Shirai et al.

Claims 49, 57, 60, 61 and 69 have been canceled and claims 50, 51, 53, 55, 56, 58, 59, 62, 63, 66 and 68 have been amended to alter their dependency. The anticipation rejections thus are moot.

Yu et al. and Ding et al. each teach (see col. 2, lines 13-22 and 41-45 of Yu et al.; col. 1, lines 44-51 and col. 2, lines 57-62 of Ding et al.) the undesirability of using LOCOS isolation. Hsieh et al. teach (Abstract; col. 3,

line 16 et seq.) that it is an object of the invention to employ STI. Accordingly, each of these references is directed to fabrication processes using STI.

In contrast, Shirai et al. teach (see 2ND ¶ beneath "Cell structure and process technologies" heading, 2ND col., p. 27.1.1) use of a LOCOS isolation technique. Yu et al., Ding et al. and Hsieh et al. each teach away from the teachings of Shirai et al. It is improper to combine teachings from references that teach away from one another.

This legal principle is described in more detail in MPEP §2145(X)(D)(2), entitled "References Cannot Be Combined Where Reference Teaches Away From Their Combination". This MPEP section states that "It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)".

Accordingly, there is, as a matter of law, no motivation to combine the teachings of these references to arrive at the subject matter of any of Applicant's claims.

Further, simply stating a conclusion that "it would have been obvious" to combine teachings from references or to modify or augment teachings from a reference does not meet the standards for a rejection under 35 U.S.C. §103(a) as set forth in The Manual of Patent Examination Procedure at §706.02(j), entitled "Contents of a 35 U.S.C. 103 Rejection." As a result, the proposed combination does not and cannot provide the invention as recited in any of Applicant's claims and thus cannot render Applicant's claims

unpatentable. This is described in more detail below with reference to MPEP §2142, entitled "Legal Concept of Prima Facie Obviousness".

This MPEP section states that in order to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. There is no motivation identified in the references to modify the references to attempt to arrive at the subject matter of Applicant's claims.

This MPEP section also states: "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

As noted above, none of the references provide any teaching, disclosure, suggestion or motivation for Applicant's affirmative recitations of a floating gate transistor employing STI together with a hemispherical grain polysilicon floating gate or a floating gate having a roughened uppermost surface. Thus, the third prong of the test cannot be met.

As a result, there cannot possibly be a reasonable expectation of success from combining their teachings to attempt to arrive at the subject matter as recited in any of Applicant's claims. The rejection fails all three prongs of the test set forth in the MPEP for forming a prima facie case of obviousness.


This MPEP section further states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." Since neither of these prongs of the test are met at all, such can hardly be found in the prior art.

Accordingly, the unpatentability rejection of claims 50-56, 58, 59 and 62-68 is in error and should be withdrawn, and claims 50-56, 58, 59 and 62-68 should be allowed.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made.**"

In view of the foregoing, allowance of claims 50-56, 58, 59 and 62-68 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Sept. 19, 2000 By: 
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Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Inventor Theodore M. Taylor
Assignee Micron Technology, Inc.
Group Art Unit 2814
Examiner Howard Weiss
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Title: Floating Gate Transistors and Methods of Forming Floating Gate Transistors

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO
JUNE 20, 2002 OFFICE ACTION

Deletions are bracketed, additions are underlined.

In the Specification

On page 1, the Title has been amended as shown below:

Floating Gate Transistor [Transistors And Methods Of Forming Floating Gate Transistors]

In the Claims

Cancel claim 49 without prejudice.

50. (Amended) The floating gate transistor of [Claim 49] claim 52, where the floating gate only partially fills the region.

51. (Amended) The floating gate transistor of [Claim 49] claim 52, where the floating gate completely fills the region.

52. (Amended) [The floating gate transistor of Claim 49]

A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses received within and projecting outwardly from the semiconductive material, the masses having opposing sides defining a region therebetween over the semiconductive material and an active area therebetween within the semiconductive material;

a floating gate received within the region and over the active area; and

a control gate operatively over the floating gate, where the floating gate comprises a roughened uppermost surface.

53. (Amended) The floating gate transistor of [Claim 49] claim 52, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

54. (Amended) [The floating gate transistor of Claim 49]

A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses received within and projecting outwardly from the semiconductive material, the masses having opposing sides defining a region therebetween over the semiconductive material and an active area therebetween within the semiconductive material;

a floating gate received within the region and over the active area; and

a control gate operatively over the floating gate, where the floating gate comprises hemispherical grain polysilicon.

55. (Amended) The floating gate transistor of [Claim 49] claim 52, where the active area has a first cross-sectional dimension and the region has a second cross-sectional dimension, the first cross-sectional dimension being parallel to and smaller than [to] the second cross-sectional dimension.

56. (Amended) The floating gate transistor of [Claim 55] claim 52, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

Cancel claim 57.

58. (Amended) The floating gate transistor of [Claim 49] claim 52, where the active area has a first cross-sectional dimension and the region has a second cross-sectional dimension, the first cross-sectional dimension being parallel to and essentially equal to the second cross-sectional dimension.

59. (Amended) The floating gate transistor of [Claim] claim 58, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

Cancel claims 60 and 61.

62. (Amended) The floating gate transistor of [Claim 61] claim 65, where the second cross-sectional dimension is larger than the first cross-sectional dimension.

63. (Amended) The floating gate transistor of [Claim 61] claim 65, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

64. (Amended) [The floating gate transistor of Claim 63]

A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and second portions projecting outwardly from the semiconductive material, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area therebetween having a first cross-sectional dimension and the opposing sides of the second portions defining a region therebetween having a second cross-sectional dimension;

a first dielectric layer received within the region and overlying the active area;

a floating gate received within the region and overlying the first dielectric layer;

a second dielectric layer overlying the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate, where the floating gate comprises hemispherical grain polysilicon.

65. (Amended) [The floating gate transistor of Claim 61]

A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and second portions projecting outwardly from the semiconductive material, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area therebetween having a first cross-sectional dimension and the opposing sides of the second portions defining a region therebetween having a second cross-sectional dimension;

a first dielectric layer received within the region and overlying the active area;

a floating gate received within the region and overlying the first dielectric layer;

a second dielectric layer overlying the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate, where the floating gate completely fills the region and comprises a rugged outermost surface.

66. (Amended) The floating gate transistor of [Claim 61] claim 65, where the second cross-sectional dimension is essentially equal to the first cross-sectional dimension.

67. (Amended) [The floating gate transistor of Claim 66]

A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and second portions projecting outwardly from the semiconductive material, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area therebetween having a first cross-sectional dimension and the opposing sides of the second portions defining a region therebetween having a second cross-sectional dimension;

a first dielectric layer received within the region and overlying the active area;

a floating gate received within the region and overlying the first dielectric layer;

a second dielectric layer overlying the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate, where the floating gate comprises hemispherical grain polysilicon, only partially fills the region and has an essentially concave uppermost surface.

68. (Amended) The floating gate transistor of [Claim 66] claim 65, where the floating gate completely fills the region.

Cancel claim 69.

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